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EXAMINER	
SHINGLETON, MICHAEL B	
ART UNIT	PAPER NUMBER
2817	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/054,358	SENTHILKUMAR	
	Examiner	Art Unit	
	Michael B. Shingleton	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,6-25, 27-29,31-33, 35 and 37-39* is/are pending in the application.

4a) Of the above claim(s) *19-23* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,6-18,24,25,27-29,31-33,35 and 37-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/05, 07/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim 32 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 32 is dependent upon cancelled claim 30. The examiner has attempted to determine which claim applicant may have meant this claim 32 to be dependent upon but could not determine which claim was actually meant by applicant. Therefore the scope of claim 32 could not be determined.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 33 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clarke 6,337,604 (Clarke) in view of Klughart US 5,546,055 (Klughart '055) and Shenai et al. 5,914,513 (Shenai).

The only Figure of Clarke discloses a "circuitry for controlling the oscillating frequency of an oscillator" now just recited as "apparatus" in some of the claims (See column 2, around line 22 of Clarke). The circuitry/apparatus of Clarke has a plurality of on-chip capacitors C1-C6 (Note that the capacitors are part of the "integrated circuit" 3 and thus are on-chip capacitors. In fact note the term "ON-CHIP COMPONENTS" as recited by the only Figure of Clarke.). Each of these capacitors is independently selectable by a control signal D0-D5, and each of these capacitors provides a controllable amount of capacitance to the oscillator to control the oscillating frequency of the oscillator (Again see column 2, around line 22 of Clarke).

Clarke is silent on the composition of the on-chip capacitors C1-C6 and the use of biasing the source/drain junction of MOSFET capacitors.

Figure 9 of Klughart '055 discloses the use of on-chip n-depletion MOSFET load capacitors 1230 and 1232 whose source and drain are clearly connected together as is clearly illustrated. Also note that the source/drain terminal of each of these capacitors is the terminal that is connected to ground in Klughart '055.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted on-chip n-depletion MOSFET load capacitors wherein the source/drain terminal of each of the individual capacitors is the terminal that is connected to ground in place of the generic capacitors C1-C6 of Clarke wherein each of these capacitors C1-C6 has a terminal connected to ground because, as the Clarke reference is silent as to the exact composition of the capacitors one of ordinary skill in the art would have been motivated to use any art-recognized equivalent capacitor such as the well-known on-chip n-depletion MOSFET capacitors as recited by Klughart '055 for the capacitors of Clarke.

As noted in the previous office actions, the only Figure of Clarke discloses an electronic device comprising a real time clock, i.e. oscillator, for generating a system time signal "CLK OUT 5" (See the only Figure and column 2, around line 20.). The real time clock has a digitally tunable oscillator (Note the use of the set of shift registers 21.) for digitally adjusting the operating frequency of the real time clock to speed up or slow down the system time signal (See column 3, around line 45). Clarke also has a memory device 21 for storing the data representing a configuration of the digitally adjusted tunable oscillator. Claim 35 merely recites that the device generates a time signal based on the oscillating frequency of the oscillator. The "CLK OUT 5" is a time signal that is clearly based on the oscillating frequency of the oscillator in Clarke. Note that the examiner must give the broadest reasonable interpretation consistent with the specification. (See MPEP 904.01).

Shenai teaches and suggests a capacitor arrangement not unlike that of Figure 2 of the instant invention. Here two capacitors are connected in parallel with the first capacitor being a MOSFET capacitor. A bias voltage is applied to the source and drain terminals via terminal "K". The advantage to this arrangement as discussed in Shenai is that this makes the MOSFET capacitor variable and thus it can be adjusted or tuned.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have provided a series connected capacitor between the source and drain terminal(s) of the MOSFET capacitor in the combination made obvious above and provide the bias voltage to this terminal so as to allow for the varying or tuning of the individual MOSFET capacitor elements as taught by Shenai. One of ordinary skill in the art would have additionally been motivated to make the combination so as to correct for manufacturing defects in the MOSFET capacitors and to provide for a finer range of tuning of the oscillator. As to the noise is allowed to pass to ground, this is an obvious consequence of the combination made obvious above. Note that the series connected capacitor that is connected to the

MOSFET capacitor would be connected to ground and thus forming a low pass filter for the bias voltage connected thereto.

Claims 1-4, 31 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clarke 6,337,604 (Clarke) in view of Shenai et al. 5,914,513 (Shenai) and Klughart US 5,801,411 (Klughart '411).

The only Figure of Clarke discloses a "circuitry for controlling the oscillating frequency of an oscillator" now just recited as "apparatus" in some of the claims (See column 2, around line 22 of Clarke). The circuitry/apparatus of Clarke having a plurality of on-chip capacitors C1-C6 (Note that the capacitors are part of the "integrated circuit" 3 and thus are on-chip capacitors. In fact note the term "ON-CHIP COMPONENTS" as recited by the only Figure of Clarke. Each of these capacitors is independently selectable by a control signal D0-D5, and each of these capacitors provides a controllable amount of capacitance to the oscillator to control the oscillating frequency of the oscillator (Again see column 2, around line 22 of Clarke). Also note, in addition to the specific recited reasoning herein, that the same reasoning as presented in the rejection of claims 33, 35 and 36 as be rejected over Clarke in view of Ochiai applies here.

Clarke is silent on the composition of the on-chip capacitors C1-C6.

Figure 9b of Klughart '411 discloses the use of on-chip p-enhancement MOSFET capacitor 32 whose source and drain are clearly connected together as "common" i.e. conventional (See column 7, around line 18). Also note that the source/drain terminal of each of these capacitors is the terminal that is connected to ground in Klughart '411.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted on-chip p-enhancement MOSFET load capacitors wherein the source/drain terminal of each of the individual capacitors is the terminal that is connected to ground in place of the generic capacitors C1-C6 of Clarke wherein each of these capacitors C1-C6 has a terminal connected to ground because, as the Clarke reference is silent as to the exact composition of the capacitors one of ordinary skill in the art would have been motivated to use any art-recognized equivalent capacitor such as the well-known on-chip p-enhancement MOSFET capacitors as recited by Klughart '411 for the capacitors of Clarke.

Shenai teaches and suggests a capacitor arrangement not unlike that of Figure 2 of the instant invention. Here two capacitors are connected in parallel with the first capacitor being a MOSFET

capacitor. A bias voltage is applied to the source and drain terminals via terminal "K". The advantage to this arrangement as discussed in Shenai is that this makes the MOSFET capacitor variable and thus it can be adjusted or tuned.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have provided a series connected capacitor between the source and drain terminal(s) of the MOSFET capacitor in the combination made obvious above and provide the bias voltage to this terminal so as to allow for the varying or tuning of the individual MOSFET capacitor elements as taught by Shenai. One of ordinary skill in the art would have additionally been motivated to make the combination so as to correct for manufacturing defects in the MOSFET capacitors and to provide for a finer range of tuning of the oscillator. As to the noise is allowed to pass to ground, this is an obvious consequence of the combination made obvious above. Note that the series connected capacitor that is connected to the MOSFET capacitor would be connected to ground and thus forming a low pass filter for the bias voltage connected thereto.

As it relates to claim 2, Clarke and Ochiai are both silent on selection of the frequency changing capacitors to be different from each other. This is merely the selection of the optimum or workable range. The chosen values of individual capacitors is a result effective variable. This selection involves but routine skill in the art and accordingly it would have been obvious to one of ordinary skill in the art at the time the invention was made to select the capacitance values to be any value within the optimum or workable range so as to shift the frequency in a controllable predetermined stepwise manner. For example the selection of the chosen values could be done in such a way that an exponential increase in capacitance can be achieved. How much the capacitance is increases for each step is dependent on the where the device is being used in or with. Accordingly, one of ordinary skill would have additionally been motivated to change the capacitance values to be different from each other because the selection of these result effective variables merely selects how fast the frequency is to increase or decrease.

Claim 31 recites that the P-type enhancement mode MOSFET will be driven into saturation. Clarke is silent on this.

However, this involves but routine skill in the art because it is merely the selection of the optimum or workable range. The selection of biasing of a MOSFET is merely a result effective variable. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select the voltage level to be such that the P-type enhancement mode MOSFET made obvious in the above combination will be operated in saturation as this is merely the selection of a result effective variable that involves but routine skill in the art.

One terminal of the capacitors is connected to a first terminal and the other terminal of the capacitors is connected to the filtered voltage is an obvious consequence of the combination made obvious above.

Claims 37 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clarke, Shenai and Klughart '411 as applied to claims 1-4, 31 and 39 above, and further in view of Horn "Basic Electronics Theory" 4th Edition pp 377-378, pp 418-426 and pp 454-465.

The reasoning as applied above in the rejection of claims 1-4,30-32 and 34 and the following:

Clearly Clarke is for a larger system. Clarke is a component of a larger system. Note that the output of Clarke is a clock. Clarke is silent on the system to be used with the clock of Clarke.

Horn describes the basic well-known use of a clock is in the structure of a computer. Horn describes the speed of the computer that as known by those of ordinary skill this is describing the oscillator or "real time clock" that is inherently within the computer. Also within a computer, computers inherently have a system time signal that represents at least one of hour, minute and second and this is the clock signal itself. For example 100 clock pulses will represent X number of seconds, etc.. Note that software will take this will take this and display on a monitor the hours, minutes and seconds of a day but the claims only requires a system time signal that represents at least one of hour, minute and second.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the clock made obvious above involving Clarke in a computer arrangement that generates a times signal that represents at least one of hour, minute and second which is based on the clock of the computer arrangement because, as the references are silent on the exact use of the component one of ordinary skill would have been motivated to use the component in any system that employs conventional clocks as part of its system such as the conventional computer arrangement of Horn that forms a system time signal that represents at least one of hour, minute and second.

Claims 13, 15, 16, 24, 25, and 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horn "Basic Electronics Theory" 4th Edition pp 377-378 and pp 454-465 in view of Clarke US 6,337,604 (Clarke).

Beginning on page 420 of Horn, Horn describes the basic well-known structure of a computer. Horn describes the speed of the computer that as known by those of ordinary skill this is describing the oscillator or "real time clock" that is inherently within the computer. Also within a computer, computers inherently have a system time signal that represents at least one of hour, minute and second and this is the clock signal itself. For example 100 clock pulses will represent X number of seconds, etc.. Note that

software will take this will take this and display on a monitor the hours, minutes and seconds of a day but the claims only requires a system time signal that represents at last one of hour, minute and second. Horn is silent on the specifics of the oscillator or real time clock or just clock.

The single Figure of Clarke discloses a circuitry for controlling the oscillating frequency of an oscillator (See column 2, line 22), the circuitry having a plurality of on-chip capacitors C1-C6, each of which is independently selectable by a control signal D0-D5, and each of which provides a controllable amount of capacitance to the oscillator to control the oscillating frequency of the oscillator (See column 2, line 22).

The single Figure of Clarke also discloses an electronic device comprising a real time clock, i.e. oscillator, for generating a system time signal "CLK OUT 5" (See the only Figure and column 2, around line 20), the real time clock having a digitally tunable oscillator (Note the use of set of shift registers 21) for digitally adjusting an operating frequency of the real time clock to speed up or slow down the system time signal (See column 3, lines 45), and a memory device 21 for storing data representing a configuration of the digitally adjusted tunable oscillator.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted the conventional real time clock/oscillator circuit of Clarke for the oscillator/real time clock/clock of Horn because, as the reference is silent as the exact oscillator/clock circuit employed one of ordinary skill in the art would have been motivated to use any art-recognized equivalent switch such as the well-known, conventional oscillator/clock circuit of Clarke. One of ordinary skill in the art also would have been additionally motivated to make the combination because Clarke teaches that the real time clock can be adjusted i.e. calibrated and thus it is advantageous to make a clock adjustable so that one can adjust the clock frequency to obtain the desired frequency as taught by Clarke. Note that Clarke contains a processor and set of control signals that adjusts the frequency of the real time clock of Clarke is stored in a register 21. Also note that since Clarke senses the real time clock and Horn clearly uses this real time clock to develop the system time signal the data processing unit of Clarke processes data based on the system time signal. In other words the system time signal and the real time clock signal are related and sensing one is in effect sensing the other and thus it is an obvious consequence that the data processing unit of Clarke processes data based on the system time signal. The examiner must give the broadest reasonable interpretation to the claims consistent with the specification.

As it relates to claims like claim 15, Clarke is both silent on selection of the frequency changing capacitors to be different from each other. This is merely the selection of the optimum or workable range.

The values of individual capacitors is a result effective variable. This selection involves but routine skill in the art and accordingly it would have been obvious to one of ordinary skill in the art at the time the invention was made to select the capacitance values to be any value within the optimum or workable range so as to shift the frequency in a controllable predetermined stepwise manner. One would have additionally bee motivated to do so because the selection of these result effective variables merely selects how fast the frequency is to increase or decrease. In other words given the desire to increase the frequency to follow an exponential curve the steps changes in capacitance could not be equal. They would need to be changed in value accordingly which is within the skill of one or ordinary skill in the art.

Claims like claims 28 and 29 recites the frequency of oscillation as being equal to 32.768 KHz. This involves but routine skill in the art because it is merely the selection of the optimum or workable range. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select the frequency to be 32,768 KHz as this involves but routine skill in the art. Additionally, one of ordinary skill in the art would have been motivated to provide any workable frequency as this is mere a selection of the result effective variable which determines how fast the microprocessor will operate.

Claims 14, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horn "Basic Electronics Theory" 4th Edition pp 377-378 and pp 454-465 in view of Clarke US 6,337,604 (Clarke) as applied to claims 13, 15, 16, 24, 25 and 27-29 above, and further in view of Theus et al. US 5,805,029 (Theus).

All the same reasoning as applied in the 35 USC 102 rejection of claims 13, 15, 16, 24, 28 and 29 following: Clarke describes in generic terms element 7 as comparing the system time signal CLK OUT 5 to be within a certain frequency range. Clarke, however, is silent on the specifics of such a structure. Note that Clarke saves the data representing the setting of the control signals in memory device 21.

Figure 4 of Theus discloses specific conventional means to compare the system time signal to the reference time signal so that a control signal can be generated to the controller of an oscillator circuit that utilizes the switching of capacitors to change the oscillator frequency. Specifically, Theus discloses receiving a reference time signal 8a and comparing this reference time signal to the system time signal 2a via a comparator 7. This controls which subsets of capacitors C11, C21, C1n, C2n that are connected to the oscillator. Note that the reference time signal just like the system time signal of Clarke represents at last one of hour, minute and second for X number of clock pulses would represent some number (including fractions) of hour(s), minute(s) and second(s).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted the conventional means of Theus to compare the reference time

signal to a system time signal so as to control generate the control signal because, as the Clarke reference is silent on the specific structure of the comparison arrangement 7 one of ordinary skill in the art would have been motivated to use any art-recognized equivalent frequency control means would have been usable such as the well-known conventional arrangement of Theus.

As to a communication port for the reference time signal, there is clearly a node and given the broadest reasonable interpretation of the claims consistent with the specification this node of Theus is seen as meeting this limitation. However, alternately it is well known in the art to provide separate ports so as that an external oscillator can be connected. This is what is sometimes called a calibrating source.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a separate port for the reference time signal in the combination made obvious above. One would have been motivated to do so, so that an accurate calibration signal, i.e. reference time signal can be used to accurately adjust the oscillator.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Horn and Clarke as applied to claims 13, 15, 16, 24, 25, and 27-29 above, and further in view of Morand et al. 6,734,483 (Morand).

All the same reasoning as applied in the above rejection of claims 13, 15, 16, 24, 25 and 27-29 and the following: Clarke is silent on the composition of the on-chip capacitors C1-C6.

Column 1 around line 19 Morand discloses poly capacitors as prior art for use in integrated circuits.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted on-chip poly capacitors in place of the generic capacitors C1-C6 of Clarke because, as the Clarke reference is silent as to the exact composition of the capacitors one of ordinary skill in the art would have been motivated to use any art-recognized equivalent capacitor such as the well-known poly capacitor as recited by Morand for the capacitors of Clarke.

Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clarke, Shenai and Klughart '411 as applied to claims 1-4, 31 and 39 above, and further in view of Kuhn Jr. US 3,930,169 (Kuhn, Jr.).

All the same reasoning as applied in the 35 USC 103 rejection of claims 1-4, 31 and 39 above and the following: Clarke is silent on the composition of the switches 9, 11, 13, 15, 17, 19(a,b) that switches the capacitors in and out of the circuit so as to change the frequency of the oscillator.

Transmission gate switches are conventional switching means as noted by Kuhn, Jr. (See Figure 1 and column 4, lines 3-29).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted conventional transmission gate switches in place of the generic switches of Clarke because, as the reference is silent as the exact switching element employed one of ordinary skill in the art would have been motivated to use any art-recognized equivalent switch such as the well-known, conventional transmission gate switch as taught by Kuhn, Jr..

As it relates to claim 8, the circuit of Clarke has a "set of registers" 21 to provide the control signals D0-D5 for selecting the individual capacitors C1-C6.

Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clarke, Shenai, Klughart '411 and Kuhn, Jr. as applied to claims 1-4, 7, 8, 31 and 39 above, and further in view of Horn "Basic Electronics Theory" 4th Edition pp 377-378, pp 418-426 and pp 454-465.

All the same reasoning as applied in the 35 USC 103 rejection of claims 1-4, 7, 8, 31 and 39 above and the following: As it relates to claim 9, Clarke is silent on using buffer circuitry to decouple the transmission gate switches from the set of memory registers.

Horn teaches that buffers are used to ensure that the output drive is sufficient to drive the devices on the output thereof.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize a buffers between the transmission gate switches and the memory registers so as to insure that there is sufficient drive for the transmission gate switches as taught by Horn.

As it relates to claim 10, Clarke is likewise silent on the use of filtered power signals to power the buffer circuitry. Buffer circuitry requires a power supply as is well known in the art so that it can provide the sufficient drive as noted above. Horn teaches that it is commonplace to utilize filtered power supplies, in particular note pages 456 and 460 to power electronic devices. This as Horn recognizes reduces "ripple", i.e. noise, or voltage fluctuations that then in turn causes less vacillations in the devices powered by such power supplies.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a filtered power supply to power the buffers made obvious above so as to reduce the introduction of noise in the system as is taught by Horn.

Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clarke, Klughart '411 and Ochiai as applied to claims 1-4, 31 and 39 above, and further in view of Leduc et al. US 6,400,231 (Leduc)

All the same reasoning as applied in the 35 USC 103 rejection of claims 1-4, 31 and 39 and the following: As it relates to claim 11, Clarke is silent on the use of an inverting amplifier as the element

that provides the gain in the oscillator. Clarke utilizes the well-known differential amplifier circuit to provide gain in a crystal oscillator. However, Leduc utilizes an inverting amplifier to provide gain for the oscillator (See column 2, lines 61-62), which is an art recognized equivalent well-known way to provide gain for a crystal oscillator.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the well known differential gain arrangement of Clarke with an inverting amplifier arrangement as these are art recognized equivalent ways to provide gain to a crystal oscillator as taught by Leduc.

As it relates to claim 12, note that the single Figure of Clarke clearly shows the plurality of frequency changing capacitors as being composed of a first subset of the plurality of capacitors that is selectively electrically coupled to a first terminal of the resonator 1, and a second subset of the plurality of capacitors that is selectively electrically coupled to a second terminal of the resonator. Note that this is just giving the broadest reasonable interpretation to the claimed invention (See MPEP 904.01).

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. Shingleton whose telephone number is (571) 272-1770.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal, can be reached on (571)272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306 and after July 15, 2005 the fax number will be 571-273-8300. Note that old fax number (703-872-9306) will be service until September 15, 2005.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MBS
September 11, 2005

Michael B Shingleton
Primary Examiner
Group Art Unit 2817